REMARKS

Claims 1 to 20 are in the present application. Claims 8 to 11 and 14 have been amended, and claims 19 and 20 have been added, all of which are fully supported by the specification, claims and drawings as originally filed.

Reconsideration of the Examiner's decisions and reexamination of this application are respectfully requested.

Objections to the claims:

Claims 10 and 13 have been objected to by the Examiner as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 10 has been amended by incorporating all of the limitations of claims 8 and 9 (the claims from which claim 10 depends). Accordingly, claim 10 should be allowable. Since claim 13 depends directly from claim 10, no amendment to claim 13 should be necessary and claim 13 should also be allowable.

The §102 rejections:

I. Claims 1 to 6 have been rejected by the Examiner under 35 USC §102(b) as being anticipated by Takeuchi et al. U.S. Patent 6,046,940 (hereafter "Takeuchi").

With respect to claim 1, the Examiner alleges that Takeuchi in Figure 22 discloses all of the features of claim 1 including the alternate arrangement of the bit line pairs and memory cells with respect to the aligned sense amplifiers.

Applicants submit that Takeuchi does not disclose this alternating arrangement. As shown in Figure 5 and described in [0029] of Applicants' specification, the bit line pairs are alternately arranged with respect to the aligned sense amplifiers. As an example, in Figure 5, sense amplifier 10 is connected to upper bit line pair 11, sense amplifier 12 is connected to lower bit line pair 13 while sense amplifier 14 is connected to upper bit line pair 15. Comparing Applicants' invention with Figure 22 of Takeuchi, it can be seen that the bit line pairs of Takeuchi are all to the left of the sense amplifiers. Thus, there is no alternate arrangement between the bit line pairs and sense amplifiers in Figure 22 of Takeuchi. Therefore, Takeuchi cannot anticipate Applicants' claim 1.

Claim 19 is new and is similar to claim 1 except that the alternate arrangement is spelled out in more detail. It is submitted that claim 19 should be allowable over Takeuchi.

Inasmuch as claims 2 to 6 depend, directly or indirectly, from claim1, and since claim 1 is believed to be allowable, then claims 2 to 6 should be allowable as well.

II. Claim 7 has been rejected by the Examiner under 35 USC §102(b) as being anticipated by Takeuchi.

With respect to claim 7, the Examiner similarly alleges that Takeuchi in Figure 22 discloses all of the features of claim 7 including the alternate arrangement of the bit line pairs and memory cells with respect to the aligned sense amplifiers and further including Q lines of P sense amplifiers where Q and P are both more than 3.

Applicants submit that Takeuchi does not disclose this alternating arrangement. As Applicants explained with respect to claim 1, all of the bit lines shown in Figure 22 of Takeuchi are to the left of the sense amplifiers. Therefore, Takeuchi cannot show any of the alternate arrangement claimed by Applicants. Moreover, Applicants require that there be Q lines of sense amplifiers where Q is more than 3. Takeuchi clearly shows in Figure

22 only 1 line of sense amplifiers. Accordingly, Takeuchi cannot anticipate Applicants' claim 7.

Claim 20 is new and is similar to claim 7 except that the alternate arrangement is spelled out in more detail. It is submitted that claim 20 should be allowable over Takeuchi.

III. Claims 8, 9, 11 and 12 have been rejected by the Examiner under 35 USC §102(b) as being anticipated by Ong et al. U.S. Patent 5,999,480 (hereafter "Ong").

With respect to claim 8, the Examiner alleges that Ong in Figure 14 discloses all of the features of Applicants' claim 8 including the alternate arrangement of the bit line pairs and memory cells with respect to the aligned sense amplifiers. Key to the rejection is the Examiner's assumption that "Ong et al. disclose only a portion of the array with regard to figure 14".

Claim 8 has been amended to clarify the alternating arrangement of the memory cells, bit line pairs and sense amplifiers. Applicants submit that Ong does not disclose the alternating arrangement claimed by Applicants in claim 8. In Ong, all of the bit line pairs extend between K and K-1 (or K+1) lines of sense amplifiers whereas Applicants bit line pairs extend at least between K and K-1 for some of the bit line pairs and K and K+1 for the other of the bit line pairs in an alternating arrangement. Further, there are Q lines of sense amplifiers in Applicants' invention wherein Q is more than 3. In Ong, there are only 2 lines of amplifiers. While Ong may only show part of the array in Figure 14, there is no disclosure in Ong that shows bit line pairs extending between K and K-1 for some of the bit line pairs and K and K+1 for the other of the bit line pairs in alternating fashion as Applicants have claimed. Accordingly, Ong cannot anticipate Applicants claim 8.

Inasmuch as claims 9, 11 and 12 depend from claim 8, and since claim 8 is believed to be allowable, then claims 9, 11 and 12 should be allowable as well.

IV. Claim 14 has been rejected by the Examiner under 35 USC §102(b) as being anticipated by Ong.

With respect to claim 14, the Examiner similarly alleges that Ong in Figure 14 discloses all of the features of Applicants' claim 14 including the alternate arrangement of the bit line pairs and memory cells with respect to the aligned sense amplifiers. Key to the rejection is the Examiner's assumption that "Ong et al. disclose only a portion of the array with regard to figure 14".

Claim 14 has been amended to clarify the alternating arrangement of the memory cells, bit line pairs and sense amplifiers. Applicants submit that Ong does not disclose the alternating arrangement claimed by Applicants in claim 14. In Ong, all of the bit line pairs extend between K and K-1 (or K+1) lines of sense amplifiers whereas Applicants bit line pairs extend at least between K and K-1 for some of the bit line pairs and K and K+1 for the other of the bit line pairs in an alternating arrangement. Further, there are Q lines of sense amplifiers in Applicants' invention wherein Q is more than 6. In Ong, there are only 2 lines of amplifiers. While Ong may only show part of the array in Figure 14, there is no disclosure in Ong that shows bit line pairs extending between K and K-1 for some of the bit line pairs and K and K+1 for the other of the bit line pairs in alternating fashion as Applicants have claimed. Accordingly, Ong cannot anticipate Applicants claim 14.

Allowable subject matter:

The Examiner's allowance of claims 15 to 18 is acknowledged.

Summary:

In view of all of the preceding remarks, it is submitted that all of claims 1 to 20 are in condition for allowance. If the Examiner finds this application deficient in any respect, the Examiner is invited to telephone the undersigned at the Examiner's earliest convenience to resolve such deficiency.

Respectfully Submitted,
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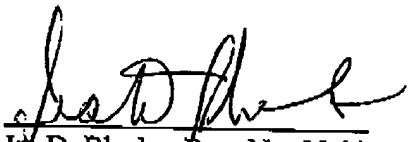

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